Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.050”**

**.050”**

**G**

**SOURCE**

**CHIP BACK IS DRAIN**

**Top Material: Al**

**Backside Material: Ag**

**Bond Pad Size: S = .008” X .010” G = .005” X .006”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 8/25/21**

**MFG: ZETEX THICKNESS .010” P/N: ZVN4424A**

**DG 10.1.2**

#### Rev B, 7/19/02